REMARKS/ARGUMENTS

Amendments were made to the specification to correct errors and to clarify the specification. No new matter has been added by any of the amendments to the specification.

Claims 1-25 are pending in the present application. Claims 1, 4, 10, 13, 16, 18, 21, 24 and 25 are amended. Reconsideration of the claims is respectfully requested.

I. Information Disclosure Statement

The Examiner has objected to the Information Disclosure Statement as filed "because it does not include a concise explanation of the relevance" of each document. Respectfully, there is no requirement in 37 CFR 1.98(a)(3) or elsewhere that would require such a submission. The Applicants have fully complied with the requirements of submitting an Information Disclosure Statement as outlined in 37 CFR 1.98. It is the Applicants' opinion that no additional disclosure is necessary.

II. Specification

The examiner has objected to the specification as needing to be readjusted to provide current U.S. Application Numbers. In response, an amended cross reference paragaph containing the requisite information is submitted herewith.

III. Double Patenting

III.A. Claims 1, 13, and 21

The Examiner has provisionally rejected claims 1, 13, and 21 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 3, 20, and 25 of co-pending Application No. 10/675,777 (hereinafter '777).

Applicants acknowledge that this is a provisional rejection. As of the date of this response, neither the rejected claims, nor the claims of the co-pending application have been allowed. Therefore a terminal disclaimer would be premature at this point. Should the Examiner indicate that either the rejected claims, or the reference be allowable, a terminal disclaimer will be filed at that time.

III.B. Claims 1, 13, and 21

The Examiner has provisionally rejected claims 1, 13, and 21 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 9, 19, 23, and 25 of co-pending Application No. 10/675,778 (hereinafter '778).

Applicants acknowledge that this is a provisional rejection. As of the date of this response, neither the rejected claims, nor the claims of the co-pending application have been allowed. Therefore a terminal disclaimer would be premature at this point. Should the Examiner indicate that either the rejected claims, or the reference be allowable, a terminal disclaimer will be filed at that time.

III.C. Claims 1, 13, and 21

The Examiner has provisionally rejected claims 1, 13, and 21 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 9, and 17 of co-pending Application No. 10/675,721 (hereinafter '721).

Applicants acknowledge that this is a provisional rejection. As of the date of this response, neither the rejected claims, nor the claims of the co-pending application have been allowed. Therefore a terminal disclaimer would be premature at this point. Should the Examiner indicate that either the rejected claims, or the reference be allowable, a terminal disclaimer will be filed at that time.

III.D. Claims 1, 10, 13, 18, 21 and 25

The Examiner has provisionally rejected claims 1, 10, 13, 18, 21 and 25 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2 and 16 of co-pending Application No. 10/675,872 (hereinafter '872).

Applicants acknowledge that this is a provisional rejection. As of the date of this response, neither the rejected claims, nor the claims of the co-pending application have been allowed. Therefore a terminal disclaimer would be premature at this point. Should the Examiner indicate that either the rejected claims, or the reference be allowable, a terminal disclaimer will be filed at that time.

III.E. Claims 10, 18, and 25

The Examiner has provisionally rejected claims 10, 18, and 25 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 9, and 17 of co-pending Application No. 10/682,385 (hereinafter '835).

Applicants acknowledge that this is a provisional rejection. As of the date of this response, neither the rejected claims, nor the claims of the co-pending application have been allowed. Therefore a terminal disclaimer would be premature at this point. Should the Examiner indicate that either the rejected claims, or the reference be allowable, a terminal disclaimer will be filed at that time.

IV. Claim Objections

The examiner has objected to claims 4, 16, and 24 as being uninterpretable "with regard to the accepted meaning of an instruction cache," or noncommensurate "with the teaching about the counter relationship with this cache in the Disclosure."

By the present Amendment, claims 4, 16 and 24 have been amended to delete "by an instruction cache." The claims are now believed to be clear and definite and withdrawal of the objection is respectfully requested.

V. 35 U.S.C. § 101

The examiner has rejected claims 1-25 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter. Claims 1, 10, 13, 18, 21, and 25 have been amended accordingly to overcome the rejection. Support for the amendments can be found on pages 64 of the as-filed specification. Providing a count of a number of times a certain instruction is executed or a memory location is accessed is a tangible result that satisfies the requirements of 35 U.S.C. § 101, and withdrawal of the rejection is respectfully requested.

VI. 35 U.S.C. § 112, Second Paragraph

The examiner has rejected claims 4, 16 and 24 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the

subject matter, which applicants regard as the invention. This rejection is respectfully traversed.

As indicated above, claims 4, 16 and 24 have been amended to delete "by an instruction cache." The claims are now believed to be clear and definite throughout.

Therefore the rejection of claims 4, 16 and 24 under 35 U.S.C. § 112, second paragraph has been overcome.

VII. 35 U.S.C. § 102, Anticipation

The examiner has rejected claims 1-25 under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 7,752,062 to Gover et al. (hereinafter "*Gover*"). This rejection is respectfully traversed.

With regard to claim 1, the Examiner states:

> As per claim 1, *Gover* discloses a method in a data processing system for monitoring execution of instruction, the method comprising: determining whether an instruction is associated with an indicator (E.g. Fig. 5; *count number , bit fields, MMCRO* – col. 10, lines 31-35; Fig. 6A; col. 11, line 62 to col. 12, line 42); and incrementing a counter associated with the instruction (e.g. *even... to be recorded/counted, counter... selection, counter freeze* – col.8, lines 41-50; col. 10, lines 53-63; col. 11 lines 14-50) in response to detecting execution of the instruction and to a determination that the instruction is associated wit the indicator.

Office Action dated March 6, 2007, p. 10.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). In this case each and every feature of the presently claimed invention is not identically shown in the cited reference, arranged as they are in the claims.

Gover describes an example of a trace technique similar to those known to the applicant and described as prior art on page 4 of the application as filed. These trace techniques are described as:

> periodically sampling a program's execution flows to identify certain locations in the program in which the program appears to spend large amounts of time. This technique is based on the idea of periodically interrupting the application or data processing system execution at regular intervals, so-called sample-based profiling. At each interruption, information is recorded for a predetermined length of time or for a predetermined number of events of interest. For example, the program counter of the currently executing thread, which is an executable portion of the larger program being profiled, may be recorded during the intervals. These values may be resolved against a load map and symbol table information for the data processing system at post-processing time, and a profile of where the time is being spent may be obtained from this analysis.

Specification, p. 4, ll. 3-19.

As described in *Gover*:

> a history of events is gathered in a processing system. The historical data is collected in a manner that is noninvasive to the system's operation but occurs within the processor. Thus, the data is unbiased and unaffected by external test instruments, while obtaining a cycle by cycle history of events during processing. Further, a straightforward manner of specifically choosing the instructions that initiate and complete monitoring activity is also obtained, which is normally more difficult in a processing system.

Gover, col. 3, ll. 44-52.

> Performance monitor 50, in a preferred embodiment, is a software-accessible mechanism intended to provide detailed information with significant granularity concerning the utilization of PowerPC instruction execution and storage control. Generally, the performance monitor 50 includes an implementation-dependent number (e.g., 2-8) of counters 51, e.g, PMC1-PMC8, used to count processor/storage related events.

Gover, col. 8, ll. 19-26.

> In operation, a notification signal is sent to PM 50 from time base facility 52 when a predetermined bit is flipped. The PM 50 then saves the machine state values in special purpose registers. In a different scenario, the PM 50 uses a "performance monitor" interrupt signalled by a negative counter (bit zero on or "1") condition.

Gover, col. 9, ll. 21-26.

In support of the current rejection, the Examiner cites the following section from *Gover*:

> Further for those events being monitored that are time sensitive, e.g., a number of stalls, idles, etc., the count number data is collected over a known number of elapsed cycles, so that the data has a context in terms of a sampling period.

Gover, col. 10, ll. 31-35.

This section states that certain monitored events are collected in a known period of time. This allows time sensitive events to be normalized over the collected time period to ease comparison of the events. This cited section does not state that an instruction is associated with an indicator, as recited in claim 1. Instead, *Gover* teaches that the monitor mode control register is incremented based on the occurrence of an event. A register is not an instruction.

In an attempt to expedite prosecution, claim 1 has been amended to better define an "indicator." Support for the amendment can be found on page 22 and in claim 5 of the application as filed. Claim 1, as amended, is as follows:

> 1. A method in a data processing system for monitoring execution of instructions, the method comprising:
>
> determining whether an instruction contains an indicator, wherein the indicator identifies the instruction or a first memory location as one that is to be monitored by a performance monitor unit; and
>
> incrementing a counter associated with the instruction in response to detecting execution of the instruction and to a determination that the instruction is associated with the indicator, the incrementing providing a count of a number of times the instruction was executed.

Gover does not anticipate amended claim 1 because *Gover* does not teach each feature of the claim. Specifically, *Gover* does not teach that "*an instruction contains an indicator, wherein the indicator identifies the instruction or memory location as one that is to be monitored by a performance monitor unit....*"

With regards to the applicant's claim 5, the Examiner points to figures 6A and 6B of *Gover*. The Examiner states that *Gover* discloses "wherein the counter is a field in the instruction...." The Applicants disagree.

Figures 6A and 6B disclose the contents of a monitor mode control register. The control register is used to control operation of the counter. See *Gover*, col. 8, ll. 17-41. A register is not an instruction.

A register is a small amount of computer memory typically used to speed the execution of computer programs by providing quick access to commonly used values—typically, the values being calculated at a given point in time. Most, but not all, modern computer architectures operate on the principle of moving data from main memory into registers, operating on them, then moving the result back into main memory—a so-called load-store architecture.

On the other hand, an instruction is a statement that indicates an operation for the computer to perform and any data to be used in performing the operation. An instruction can be in machine language or a programming language.

Because a register is not an instruction, *Gover* does not teach each feature of claim 1. Specifically, *Gover* does not teach that "*an instruction contains an indicator, wherein the indicator identifies the instruction or memory location as one that is to be monitored by a performance monitor unit....*" *Gover* does not anticipate amended claim 1. Therefore, the rejection of claim 1 under 35 U.S.C. §102 has been overcome.

Independent claims 10, 13, 18, 21, and 25 have been amended consistent with the new features of claim 1. Therefore, by virtue of arguments similar to those presented above, *Gover* also does not anticipate claims 10, 13, 18, 21, and 25.

Claims 2-9, 11-12, 14-17, 19-20, and 22-24 depend from claims 1, 10, 13, 18, and 21 respectively. Therefore, the same distinctions between *Gover* and claims 1, 10, 13, 18, and 21 apply to the respective dependent claims. Therefore, the rejection of claims 2-9, 11-12, 14-17, 19-20, and 22-24 under 35 U.S.C. § 102 has been overcome.

VIII. Conclusion

It is respectfully urged that the subject application is patentable over *Gover* and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: June 6, 2007

Respectfully submitted,

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